查询IXFX50N50供应商

IXYS

HiPerFET™ Power MOSFETs

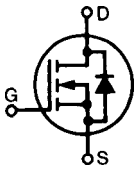
IXFX 50N50
IXFX 55N50

V_{DSS}	I_{D25}	$R_{DS(on)}$
500 V	50 A	100 mΩ
500 V	55 A	80 mΩ

$t_{rr} \leq 250$ ns

Single Die MOSFET

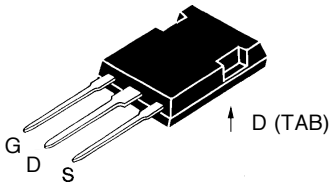
Preliminary data sheet



Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		500	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	50N50	50	A
		55N50	55	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	50N50	200	A
		55N50	220	A
I_{AR}	T_C = 25°C	50N50	50	A
		55N50	55	A
E_{AR}	T_C = 25°C		60	mJ
E_{AS}	T_C = 25°C		3	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$ $T_J \leq 150$°C, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		520	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.063 in.) from case for 10 s		300	°C
M_d	Mounting torque		1.13/10	Nm/lb.in.
Weight			6	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 1mA		500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA		2.5		4.5	V
I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0				±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$	T_J = 25°C			25	µA
	V_{GS} = 0 V	T_J = 125°C			2	mA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 0.5 I_{D25} Note 1	50N50			100	mΩ
		55N50			80	mΩ

PLUS 247™ (IXFX)



Features

- International standard package
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic rectifier

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls

Advantages

- PLUS 247™ package for clip or spring mounting
- Space savings
- High power density

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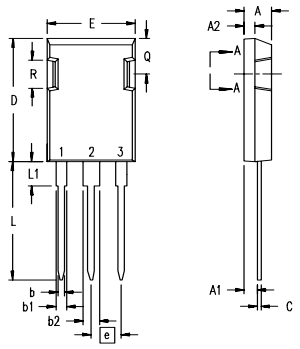
Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 I_{D25} Note 1		45		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		9400		pF
C_{oss}			1280		pF
C_{rss}			460		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25} R_G = 2 Ω (External),		45		ns
t_r			60		ns
$t_{d(off)}$			120		ns
t_f			45		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}		330		nC
Q_{gs}			55		nC
Q_{gd}			155		nC
R_{thJC}				0.22	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)		min.	typ.	max.	
I_S	V_{GS} = 0 V	55N50			55	A
		50N50			50	A
I_{SM}	Repetitive; pulse width limited by T_{JM}	55N50			220	A
		50N50			200	A
V_{SD}	I_F = I_S, V_{GS} = 0 V Note 1				1.5	V
t_{rr}	I_F =25 A,-di/dt = 100 A/µs, V_R = 100 V				250	ns
Q_{RM}				1.0		µC
I_{RM}				10		A

Note: 1.Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %

PLUS 247™ Outline



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)
4 - Drain (Collector)

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Figure 1. Output Characteristics at 25°C

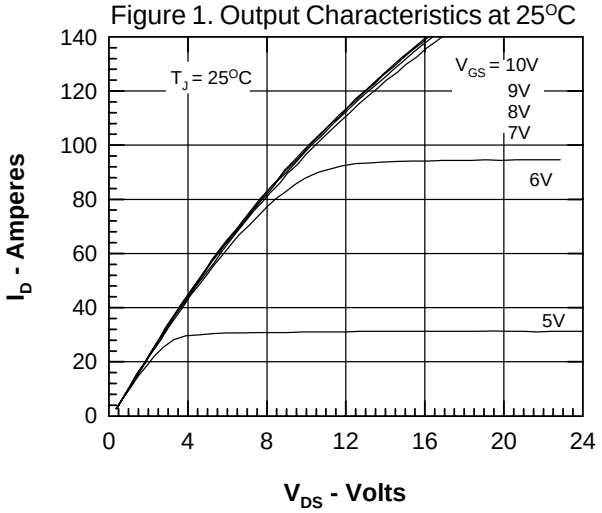


Figure 2. Output Characteristics at 125°C

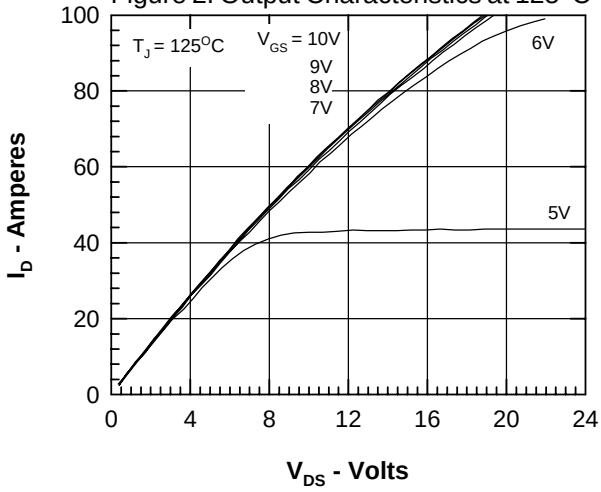


Figure 3. $R_{DS(on)}$ normalized to 0.5 I_{D25} value vs. I_D

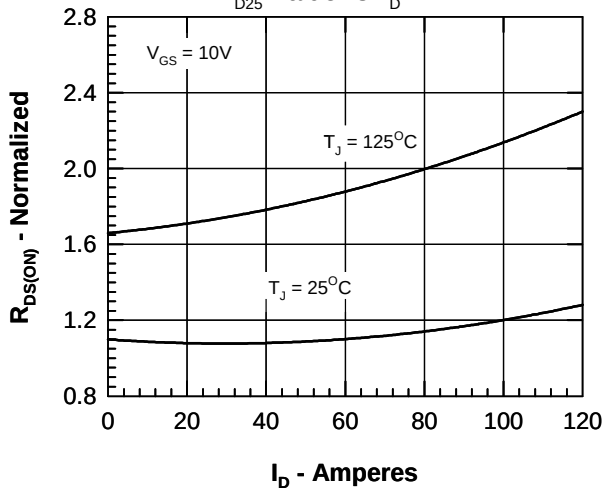


Figure 4. $R_{DS(on)}$ normalized to 0.5 I_{D25} value vs. T_J

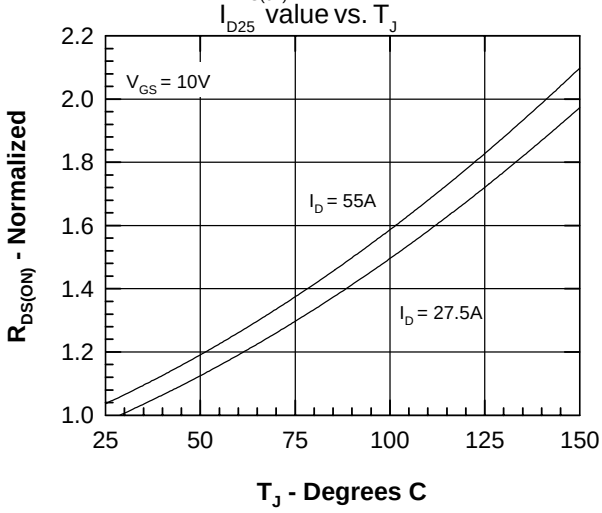


Figure 5. Drain Current vs. Case Temperature

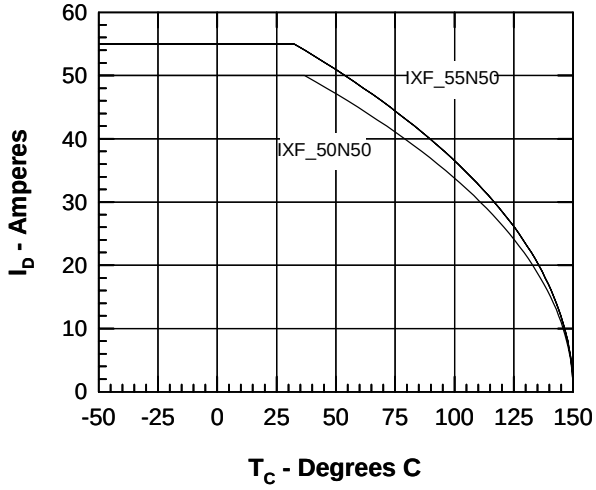


Figure 6. Admittance Curves

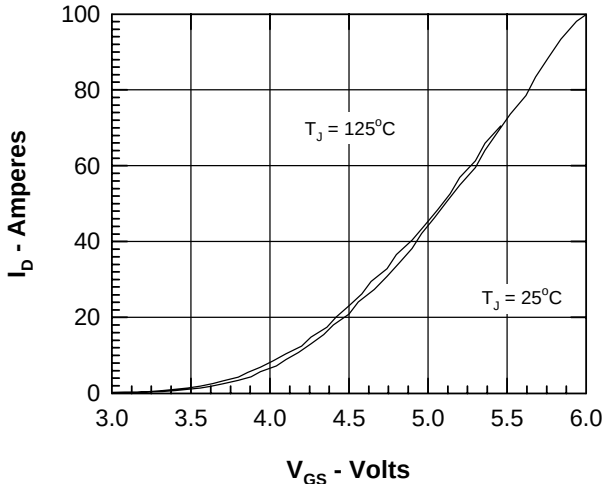


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Figure 7. Gate Charge

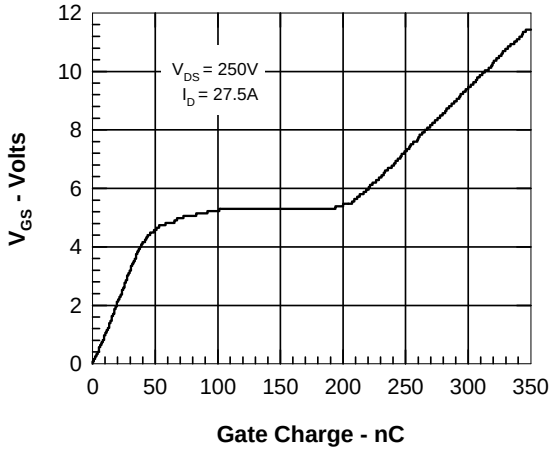


Figure 8. Capacitance Curves

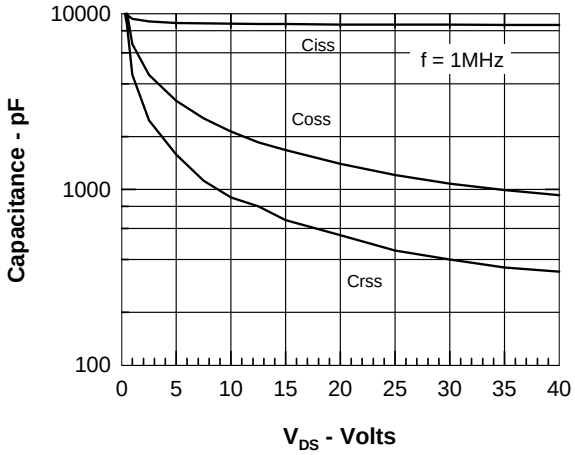


Figure 9. Forward Voltage Drop of the Intrinsic Diode

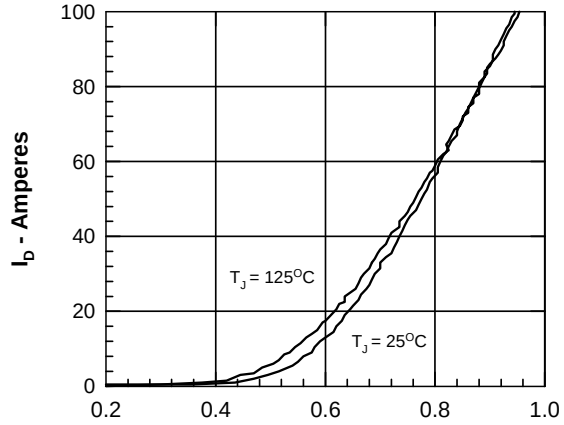
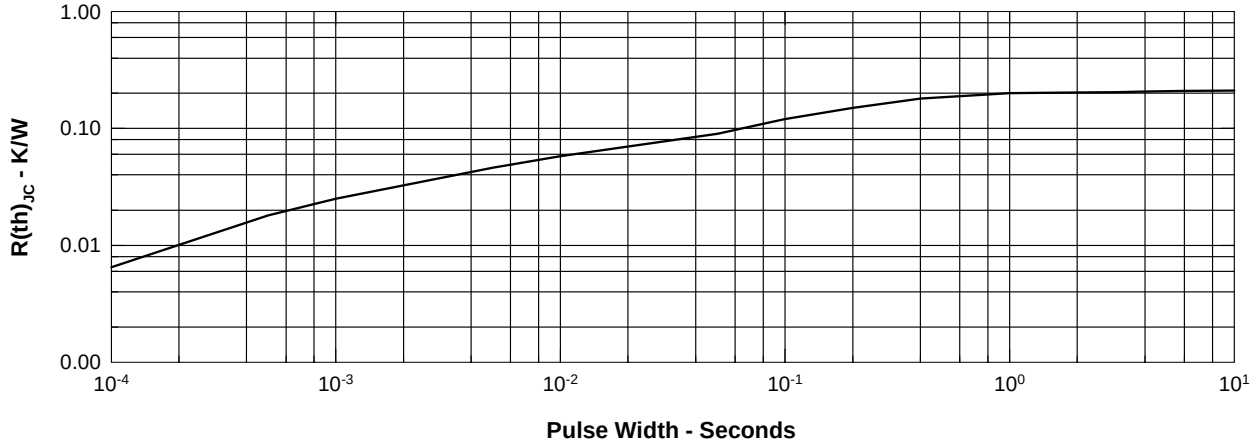


Figure10. Forward Bias Safe Operating Area



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